Amendments to the Claims:

This listing will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A circuit for controlling the direction of data traffic, between a first device and a second device, over only a single I/O line by utilizing the differences of instantaneous source impedance of [[a]] the controlling I/O line during data out and data in modes.

2. (Original) The circuit in claim 1, wherein said controlling the direction of data traffic includes the controlling of input and output data communication.

3. (Original) The circuit in claim 2, wherein said controlling of input and output data communication is without the presence of any additional signaling protocol that identifies a data input phase or a data output phase.

4. (Original) The apparatus in claim 2, wherein said controlling of input and output data communication is conducted without any non-data bit overhead.

5. (Original) The apparatus in claim 1, wherein said instantaneous source impedance is changed between a low impedance and a high impedance.

6. (Original) The apparatus in claim 5, wherein a ratio of said high impedance to said low impedance is about 1000:1.

7. (Original) The apparatus in claim 5, wherein a ratio of said high impedance to said low impedance is at least about 1000:1.

8. (Original) The apparatus in claim 5, wherein a ratio of said high impedance to said low impedance is between at least about 100:1.

9. (Original) The apparatus in claim 5, wherein a ratio of said high impedance to said low impedance is between at least about 100:1 and about 10000:1.

10. (Original) The apparatus in claim 1, wherein said first device comprises a microprocessor and said second device comprises a peripheral device.

11. (Original) The apparatus in claim 10, wherein said controlling I/O line comprises a controlling microprocessor I/O line.

12. (Original) The apparatus in claim 10, wherein said peripheral device comprises a memory.

13. (Previously presented) The apparatus in claim 10, wherein said peripheral device is a device selected from the set of devices consisting of a memory, a remote clock, a temperature sensor, a digital potentiometer, a digital audio circuit, a security circuit, a digital signal processing circuit, a controller circuit, a storage device, an analog-to-digital converter, a digital-to-analog converter, a memory storing a serial number, and combinations thereof.

14. (Original) The circuit in claim 1, wherein:

said controlling the direction of data traffic includes the controlling of input and output data communication;

said controlling of input and output data communication is without the presence of any additional signaling protocol that identifies a data input phase or a data output phase;

said controlling of input and output data communication is conducted without any non-data bit overhead;

said instantaneous source impedance is changed between a low impedance and a high impedance, and a ratio of said high impedance to said low impedance is between at least about 100:1 and about 10000:1;

said first device comprises a microporcessor and said second device comprises a peripheral device coupled with said microprocessor, and said controlling I/O line comprises a controlling microprocessor I/O line.

15. (Original) The apparatus in claim 14, wherein said peripheral device comprises a memory.

16. (Previously presented) The apparatus in claim 14, wherein said peripheral device is a device selected from the set of devices consisting of a memory, a remote clock, a temperature sensor, a digital potentiometer, a digital audio circuit, a security circuit, a digital signal processing circuit, a controller circuit, a storage device, an analog-to-digital converter, a digital-to-analog converter, a memory storing a serial number, and combinations thereof.

17. (Currently amended) An interface circuit for controlling the direction of data traffic, between a processor and a memory coupled to said processor, over only a single I/O line by utilizing the differences of instantaneous source impedance of [[a]] the controlling I/O line during data out and data in transmission modes.

18. (Original) The interface circuit of claim 17, wherein: said controlling of direction of data traffic is without the presence of any additional signaling protocol that identifies a data input phase or a data output phase; and said instantaneous source impedance is changed between a low impedance and a high impedance, and a ratio of said high impedance to said low impedance is between at least about 500:1.

19. (Original) The interface circuit of claim 17, wherein

said controlling of direction of data traffic is without the presence of any additional signaling protocol that identifies a data input phase or a data output phase;

said controlling of input and output data communication is conducted without any non-data bit overhead; and

said instantaneous source impedance is changed between a low impedance and a high impedance, and a ratio of said high impedance to said low impedance is between at least about 100:1 and about 10000:1.

20. (Original) The interface circuit of claim 17, wherein the bidirectional exchange of data occurring over a single microprocessor I/O line on a bit-by-bit basis.

21. (Original) The interface circuit of claim 17, wherein the bidirectional exchange of data occurring over a single microprocessor I/O line independent of any signaling protocol.

22. (Previously presented) The interface circuit of claim 17, wherein the bidirectional exchange of data occurring over a single I/O line on a bit-by-bit basis is independent of any signaling protocol.

23. (Original) The interface circuit of claim 1, wherein the bidirectional exchange of data occurring over a single microprocessor I/O line on a bit-by-bit basis.

24. (Original) The interface circuit of claim 1, wherein the bidirectional exchange of data occurring over a single microprocessor I/O line independent of any signaling protocol.

25. (Original) The interface circuit of claim 1, wherein the bidirectional exchange of data occurring over a single I/O line on a bit-by-bit basis independent of any signaling protocol.

26. (Original) The interface circuit of claim 1, wherein the bidirectional exchange of data occurring over a half-duplex communications line that requires no signaling protocol.

27. (Original) The interface circuit of claim 1, wherein the bidirectional exchange of data occurring over a half-duplex communications line that requires no signaling protocol.

28. (Original) The interface circuit of claim 17, wherein the bidirectional exchange of data occurring over a half-duplex communications line that requires no signaling protocol.

29. (Original) The interface circuit of claim 1, wherein the controlling of the direction of data transmission over a single conductor is accomplished without the need of timing commands.

30. (Original) The interface circuit of claim 17, wherein the controlling of the direction of data transmission over a single conductor is accomplished without the need of timing commands.

31. (Original) The interface circuit of claim 1, wherein the controlling of the direction of data transmission over a single conductor is accomplished without the need of timing circuits.

32. (Original) The interface circuit of claim 17, wherein the controlling of the direction of data transmission over a single conductor is accomplished without the need of timing circuits.

33.-38. (Canceled)

39. (Original) The circuit in claim 1, further including means for preventing a peripheral device from receiving a data as an input that is intended as an output to an external circuit.

40. (Original) The circuit in claim 39, wherein said external circuit comprises a microprocessor.

41. (Original) The circuit in claim 40, wherein said external circuit comprises a host computer or a component thereof.

42. (Original) The circuit in claim 1, further comprising data signal and clock signal separation circuit for separation of data-out + clock and data-in at the peripheral device such that it can interface to a standard SPI device.

43. (Original) The circuit in claim 17, further comprising data signal and clock signal separation circuit for separation of data-out + clock and data-in at the peripheral device such that it can interface to a standard SPI device.

44. (Original) The circuit in claim 1, further comprising a data signal extraction circuit operative to extract a data signal from a composite signal comprising said data signal and another signal.

45. (Original) The circuit in claim 44, wherein said another signal comprises a clock signal.

46. (Original) The circuit in claim 1, further comprising a clock signal extraction circuit operative to extract a clock signal from a composite signal comprising said clock signal and another signal.

47. (Original) The circuit in claim 46, wherein said another signal comprises a data signal.

48. (Original) The circuit in claim 1, further comprising a circuit for separation of data-out and data-in at the peripheral device such that it can interface to a standard UART at the peripheral device.

49. (Original) The circuit in claim 1, further comprising a circuit for separation of data-out and data-in at the peripheral device such that it can interface to a standard SPI peripheral device.

50. (Original) The circuit in claim 1, further comprising a separation circuit for separating an output data signal from an input data signal at said peripheral device.

51. (Original) The circuit in claim 1, further comprising separation means for separating an output data signal from an input data signal at said peripheral device.

52. (Original) The circuit in claim 1, wherein separation of data out and data in, at the second device, is performed such that it can interface to devices which use Pulse Width Modulation to convey analog values.